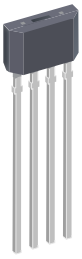
A17502

Dual Output Narrow Pitch Differential Speed and Direction Sensor IC

FEATURES AND BENEFITS

- Ideally suited for xEV asynchronous electric motor applications with narrow pitch targets
- High-speed switching bandwidth up to 40 kHz
- Two independent output channels for either speed and direction or AB outputs in quadrature
- ASIL B(D) compliant (ISO 26262), assessment pending, with optional fault detection output protocol
- Differential sensing for robustness to external magnetic disturbance
- EEPROM enabled factory traceability throughout product lifecycle
- Also available with integrated magnet (see ATS17502 datasheet)

PACKAGE:



4-Pin SIP
(suffix K)

Not to scale

DESCRIPTION

The A17502 is a single IC solution designed for rotational position sensing of a ring magnet target found in automotive and industrial electric motor applications (often with specific application and safety requirements).

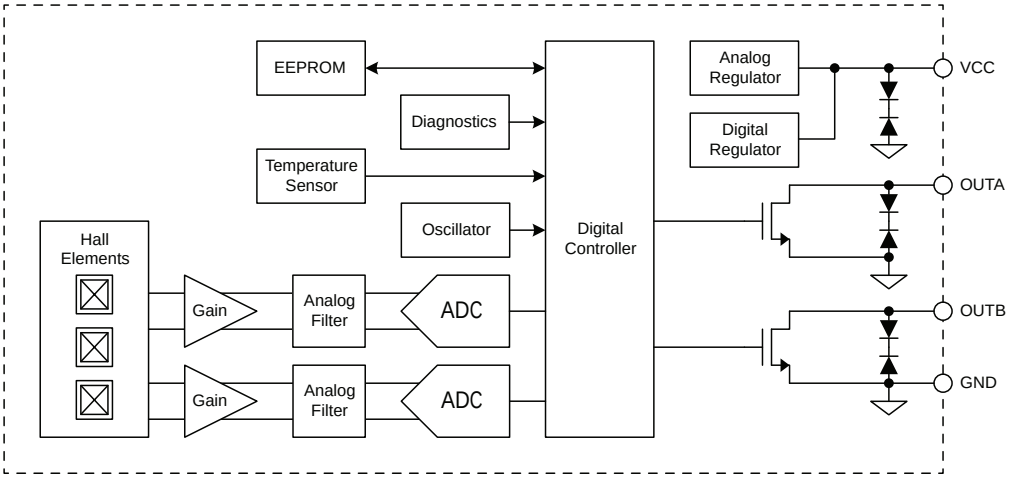
Three Hall elements are incorporated to create two independent differential channels. These inputs are processed by digital circuits and robust algorithms designed to eliminate the detrimental effects of magnetic and system offsets, and to address false output transitions caused by target vibrations in electric motors at startup and low speed operation. The differential signals are used to produce a highly accurate speed output and, if desired, provide information on the direction of rotation.

Advanced calibration techniques are used to optimize signal offset and amplitude. This calibration, combined with the digital tracking of the signal, results in accurate switch points over air gap, speed, and temperature.

The IC can be programmed for a variety of applications requiring dual-phase target speed and position signal information or simultaneous high-resolution target speed and direction information. It can be configured to enable Fault Detection mode for ASIL B(D) utilization (assessment pending).

The A17502 K package is a lead (Pb) free 4-pin SIP package with a 100% matte-tin-plated lead frame.

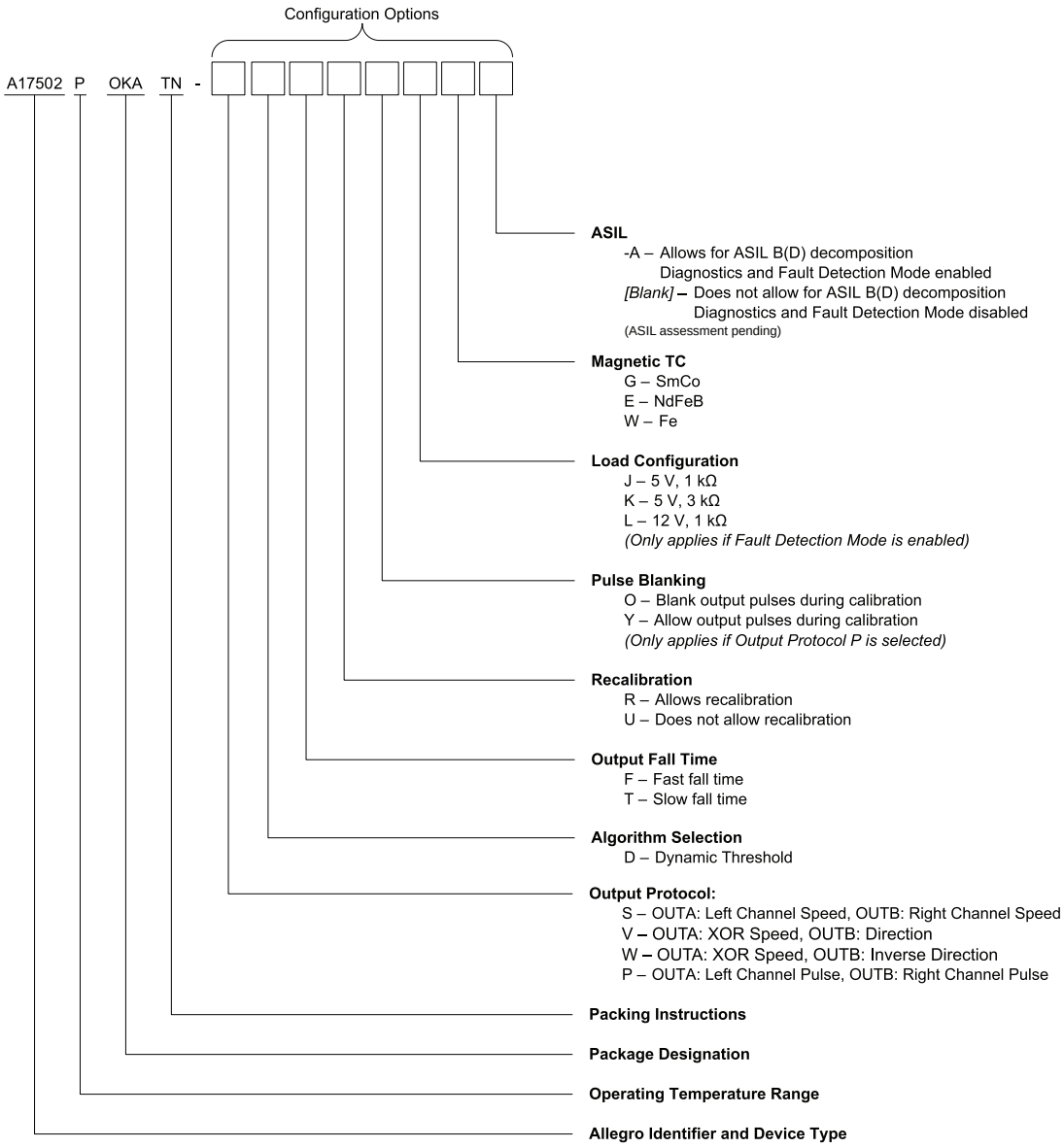
Functional Block Diagram



SELECTION GUIDE [1]

Part Number	Packing
A17502POKATN-SDFUYJE	4000 pieces per 13-inch reel

[1] Not all selectable combinations are available, contact Allegro for additional selections and packing options.



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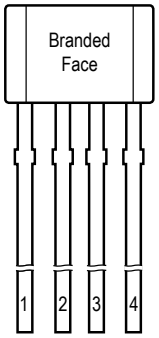
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Voltage	V_{OUT}		28	V
Reverse Output Voltage	V_{ROUT}	$R_{PULLUP} \geq 1$ kΩ	–0.5	V
Output Sink Current	I_{OUT}	Internal current limiting is intended to protect short-term output current, not intended for continuous operation.	50	mA
Operating Ambient Temperature Range	T_A		–40 to 160	°C
Junction Temperature	T_J		175	°C
Storage Temperature Range	T_{stg}		–65 to 170	°C

PINOUT DIAGRAM



K Package, 4-Pin SIP

PINOUT TABLE

Name	Pin	Function
VCC	1	Supply Voltage
OUTA	2	Configurable Output A
OUTB	3	Configurable Output B
GND	4	Ground

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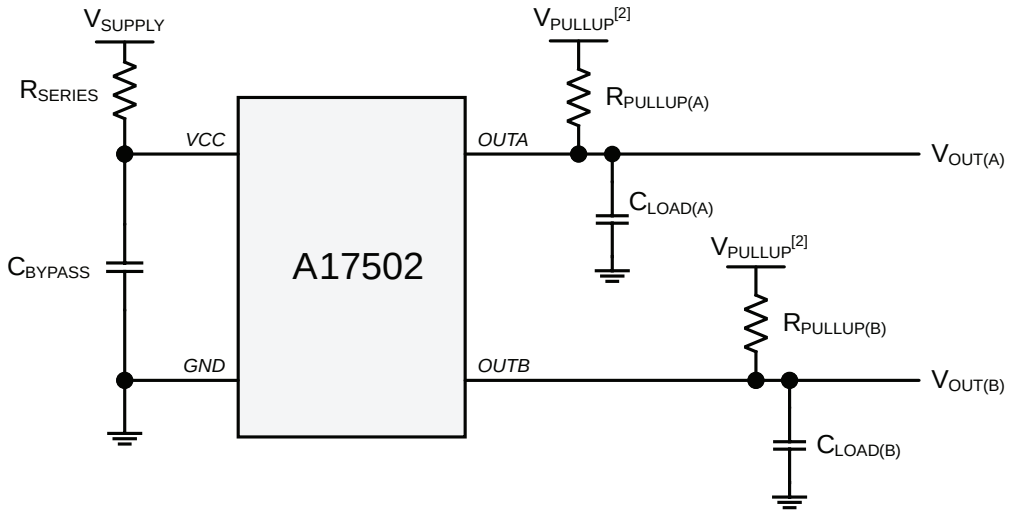
TYPICAL APPLICATION CIRCUIT



COMPONENTS [3]

Characteristic	Symbol	Notes	Value (Typ.)	Unit
Series Resistance	R_{SERIES}	Recommended for typical EMC requirements	100	Ω
OUTA Pullup Resistance	$R_{PULLUP(A)}$	Required for functional operation; recommended value dependent on programming options	1	kΩ
OUTB Pullup Resistance	$R_{PULLUP(B)}$	Required for functional operation; recommended value dependent on programming options	1	kΩ
Bypass Capacitance	C_{BYPASS}	Recommended for typical EMC requirements	100	nF
OUTA Load Capacitance	$C_{LOAD(A)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF
OUTB Load Capacitance	$C_{LOAD(B)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF

[2] V_{PULLUP} may be connected to V_{CC} if V_{CC} meets V_{PULLUP} requirements. See Operating Characteristics section.
[3] Components listed are typical recommended values and are not suited for all applications and/or programmable options. See Operating Characteristics and Selection Guide for more information.

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OPERATING CHARACTERISTICS: Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [4]	Max.	Unit
ELECTRICAL SUPPLY CHARACTERISTICS							
Supply Voltage [5]	V_{CC}	Voltage across VCC and GND		4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$			–	–	3.99	V
Supply Current	I_{CC}			–	10	15	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –18 V		–10	–	0	mA
ELECTRICAL PROTECTION CHARACTERISTICS							
Supply Clamp Voltage	$V_{CSUPPLY}$	T_A = 25°C; I_{CC} = 18 mA		28	–	–	V
Reverse Supply Clamp Voltage	$V_{RCSUPPLY}$	T_A = 25°C; I_{CC} = –3 mA		–	–	–18	V
Output Clamp Voltage	V_{COUT}	T_A = 25°C; I_{OUT} = 3 mA		28	–	–	V
Output Current Internal Limiter	$I_{OUT(LIM)}$	Current limited by design for short circuit event on OUTA and OUTB independently; low impedance output state		30	55	85	mA
POWER-ON CHARACTERISTICS							
Power-On State	POS	For OUTA and OUTB		$V_{OUT(HIGH)}$			V
Power-On Time	t_{PO}	Time from V_{CC} > $V_{CC(min)}$ to when sensor IC output is valid		–	–	1	ms
CALIBRATION CHARACTERISTICS							
First Output Edge	–	Amount of target rotation with constant direction following power-on until first electrical output transition; see Figure 1		–	1	–	T_{CYCLE}
Initial Calibration	–	Amount of target rotation with constant direction following power-on until calibration is complete; see Figure 1		–	2	–	T_{CYCLE}
OUTPUT CHARACTERISTICS [6]							
Output Low Voltage	$V_{OUT(LOW)}$	Fault Detection Mode disabled; I_{OUT} = 10 mA		–	0.165	0.35	V
		Fault Detection Mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	0.5	–	1.25	V
			12 V, 1 kΩ option	1.2	–	3.6	V
Output High Voltage	$V_{OUT(HIGH)}$	Fault Detection Mode disabled		–	V_{PULLUP}	–	V
		Fault Detection Mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	3.75	–	4.5	V
			12 V, 1 kΩ option	8.4	–	10.8	V

Continued on next page...

[4] Typical values are at T_A = 25°C and V_{CC} = 5 V unless otherwise specified. Performance may vary for individual units, within the specified maximum and minimum limits.
[5] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[6] Output characteristics are valid for each output independently, unless otherwise specified.

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OPERATING CHARACTERISTICS (continued): Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [7]	Max.	Unit
OUTPUT CHARACTERISTICS (continued) [8]							
Fault Voltage [9]	V_{FAULT}	Fault Detection Mode enabled; 5 V, 1 kΩ or 5 V, 3 kΩ option	High fault ($V_{FAULT(HIGH)}$)	4.5	–	–	V
			Mid fault ($V_{FAULT(MID)}$)	1.25	–	3.75	V
			Low fault ($V_{FAULT(LOW)}$)	–	–	0.5	V
		Fault Detection Mode enabled; 12 V, 1 kΩ option	High fault ($V_{FAULT(HIGH)}$)	10.8	–	–	V
			Mid fault ($V_{FAULT(MID)}$)	3.6	–	8.4	V
			Low fault ($V_{FAULT(LOW)}$)	–	–	1.2	V
Allowable Pullup Voltage	V_{PULLUP}	Fault Detection Mode disabled		4	–	24	V
		Fault Detection Mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	4.75	5	5.25	V
			12 V, 1 kΩ option	11.4	12	12.6	V
Allowable Pullup Resistor [10]	R_{PULLUP}	Fault Detection Mode disabled		–	1	–	kΩ
		Fault Detection Mode enabled	5 V, 1 kΩ option	0.8	–	1.46	kΩ
			5 V, 3 kΩ option	1.46	–	3.4	kΩ
			12 V, 1 kΩ option	0.9	–	1.1	kΩ
Allowable Load Capacitor [11]	C_{LOAD}	Fault Detection Mode enabled		1	–	–	nF
Output Leakage Current	$I_{OUT(OFF)}$	Fault Detection Mode disabled; $V_{OUT} = V_{OUT(HIGH)}$		–	–	10	μA
Duty Cycle	D	Speed output protocol; sinusoidal input signal; f_{OP} < 1 kHz		45	50	55	%
Output Rise Time	t_r	10%→90%; V_{PULLUP} = 5 V; R_{PULLUP} = 1 kΩ; C_{LOAD} = 2.2 nF		–	5	–	μs
Output Fall Time	t_f	90%→10%; V_{PULLUP} = 5 V; R_{PULLUP} = 1 kΩ; C_{LOAD} = 2.2 nF	Fault Detection Mode disabled; Fast fall time option	–	0.5	–	μs
			Fault Detection Mode disabled; Slow fall time option	–	3.5	–	μs
			Fault Detection Mode enabled	–	6	–	μs
Forward Pulse Width [12]	$t_{w(FWD)}$			38	45	52	μs
Reverse Pulse Width [12]	$t_{w(REV)}$			76	90	104	μs
Propagation Delay	t_d	Delay from the magnetic signal crossing a switch point threshold to the start of the output transition		–	8	–	μs
Jitter [13]	–	σ×6; sinusoidal input signal; f_{OP} = 1 kHz	$B_{DIFF(pk-pk)}$ = 100 G	–	–	0.13	target degrees
			$B_{DIFF(pk-pk)}$ = 150 G	–	–	0.115	target degrees
			$B_{DIFF(pk-pk)}$ = 200 G	–	–	0.100	target degrees

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[7] Typical values are for V_{CC} = 5 V and T_A = 25°C, unless otherwise specified, Performance may vary for individual units, within the specified maximum and minimum limits.
[8] Output characteristics are valid for each output independently, unless otherwise specified.
[9] Valid with Fault Detection Mode enabled and correct programming of the Fault Detection Load Circuit option; see Selection Guide.
[10] See Application Circuit section.
[11] Minimum capacitor required when Fault Detection Mode is enabled to ensure correct output levels over operating conditions. Increased load capacitance will directly impact maximum operating frequency due to the increased rise and fall times; see Application Circuit section.
[12] Valid only when pulse output protocols are selected. Forward and reverse rotation relative to the mechanical target rotation can be selected by Left/Right Channel Pulse or Left/Right Channel Pulse Inverted output protocols. See Output Protocol Options for more information.
[13] Guaranteed by design and characterization only. Characterization performed my measuring greater than 1,000 falling output edges of the same target feature at constant temperature using Allegro Standard 60-0 Ring Magnet. Value representative of a 6-σ distribution, such that 99.76% of the measured values are within the specified target degree.

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OPERATING CHARACTERISTICS (continued): Valid over operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [14]	Max.	Unit
SWITCH POINT CHARACTERISTICS							
Operate Point	B_{OP}	% of $B_{DIFF(PKPK)}$; $V_{OUT} = V_{OUT(LOW)} \rightarrow V_{OUT} = V_{OUT(HIGH)}$		–	70	–	%
Release Point	B_{RP}	% of $B_{DIFF(PKPK)}$; $V_{OUT} = V_{OUT(HIGH)} \rightarrow V_{OUT} = V_{OUT(LOW)}$		–	30	–	%
Hysteresis	B_{HYS}	ΔB_{DIFF} after switch point to allow next output transition; % of $B_{DIFF(PKPK)}$		–	40	–	%
INPUT CHARACTERISTICS							
Operating Frequency	f_{OP}	Sinusoidal input signal; forward and reverse target rotation; not valid for Pulse or Inverse Pulse output protocol		0	–	40	kHz
Forward Pulse Operating Frequency	$f_{OP(FWD)}$	Pulse or Inverse Pulse output protocol		0	–	9	kHz
Reverse Pulse Operating Frequency	$f_{OP(REV)}$	Pulse or Inverse Pulse output protocol		0	–	6	kHz
Operating Magnetic Input [15]	$B_{DIFF(pk-pk)}$	See Figure 2	$f_{OP} \le 20$ kHz	30	–	–	G
			$f_{OP} > 20$ kHz	40	–	–	G
Operating Magnetic Input Peak [15]	B_{DIFF}	See Figure 2		–1150	–	1150	G
Operating Magnetic Input Signal Variation [16]	$\Delta B_{DIFF(pk-pk)}$	Bounded amplitude ratio within T_{WINDOW}; no missed output transitions; possible incorrect direction information and/or reduction in switch point accuracy; see Figure 3 and Figure 4		0.6	–	2	–
Operating Magnetic Input Signal Variation Window	T_{WINDOW}	Rolling window in which $\Delta B_{DIFF(pk-pk)}$ cannot exceed bounded ratio; see Figure 3 and Figure 4		8	–	–	T_{CYCLE}
THERMAL CHARACTERISTICS							
Package Thermal Resistance	$R_{\theta JA}$	Single-sided PCB, with copper limited to solder pads		–	177	–	°C/W

[14] Typical values are for V_{CC} = 5 V and T_A = 25°C, unless otherwise specified. Performance may vary for individual units, within the specified maximum and minimum limits.
[15] Differential magnetic field is measured for Left Channel (E1-E2) and Right Channel (E2-E3) independently; see Package Diagram. Magnetic field is measured orthogonally to the branded package face.
[16] Operating magnetic input variation is valid for symmetrical peak variation about the signal offset. $B_{DIFF(pk-pk)}$ must always be greater than $B_{DIFF(pk-pk,min)}$.

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REFERENCE

Definition of Terms

T_{CYCLE}

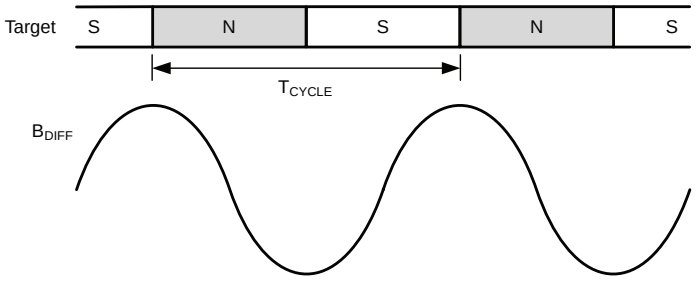

Figure 1: Definition of T_{CYCLE}

T_{CYCLE} = Target Cycle; the amount of rotation that moves one tooth and valley across the sensor.

B_{DIFF} = The differential magnetic flux density sensed by the IC.

Differential Magnetic Input

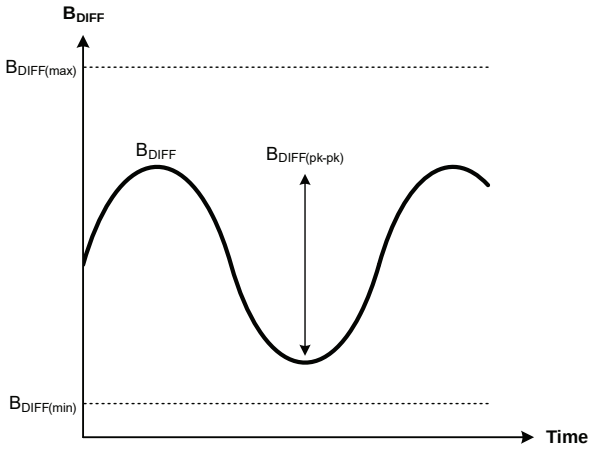

Figure 2: Differential Magnetic Input

$B_{DIFF(pk-pk)}$ = The peak-to-peak magnetic flux density sensed by the IC.

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Operating Magnetic Signal Variation and Window

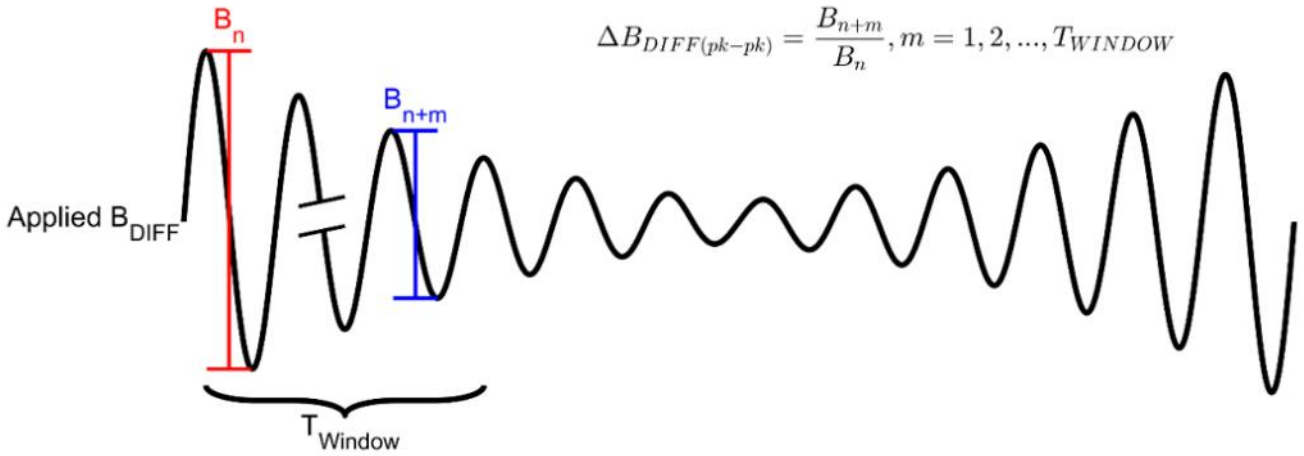

Figure 3: Repeated Period Variation

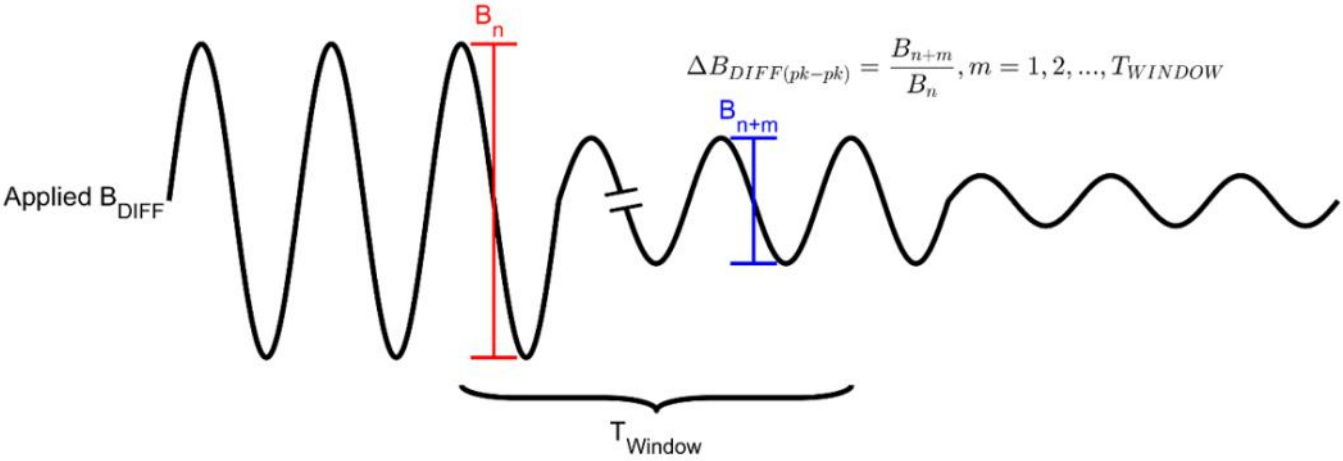

Figure 4: Single Period Variation

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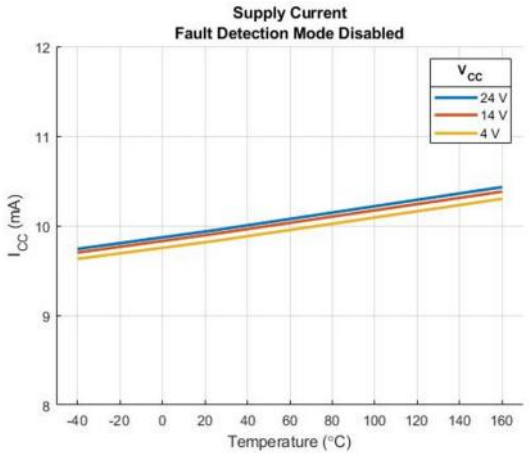
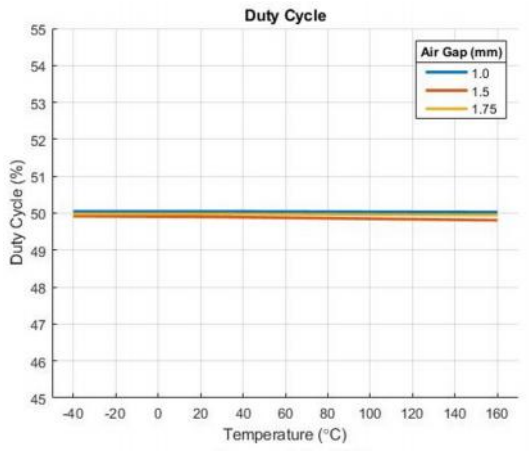
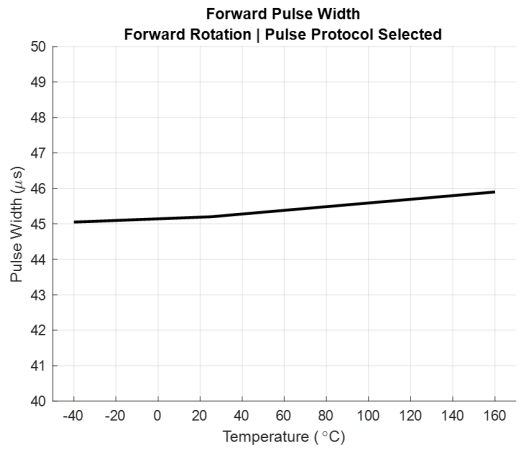
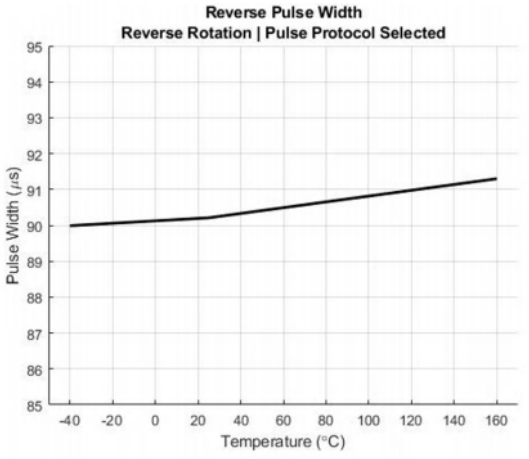
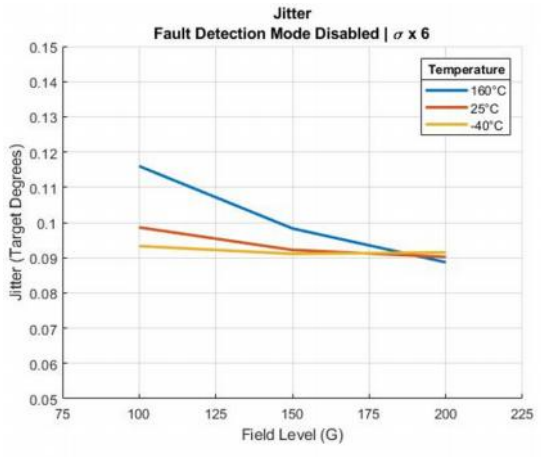
CHARACTERIZATION PLOTS [17]

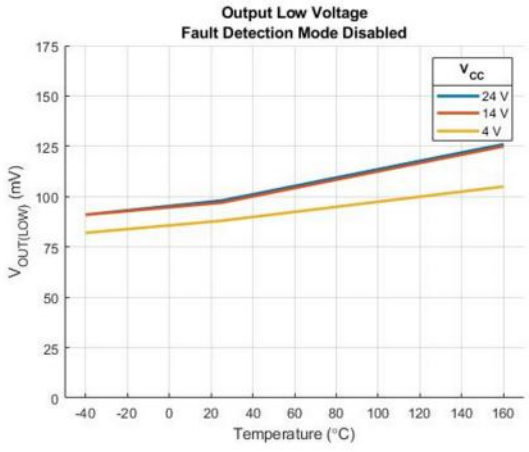












[17] Characterization data representative of distribution averages. Characterization tested at f_{OP} = 1 kHz, V_{CC} = 5 V, V_{PULLUP} = 5 V, R_{PULLUP} = 1 kΩ, and C_{LOAD} = 2.2 nF unless otherwise specified.

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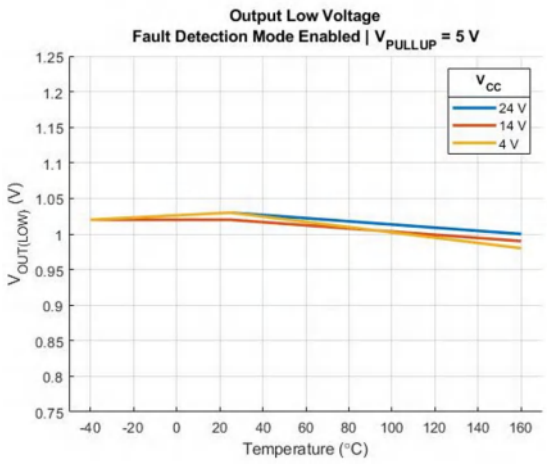

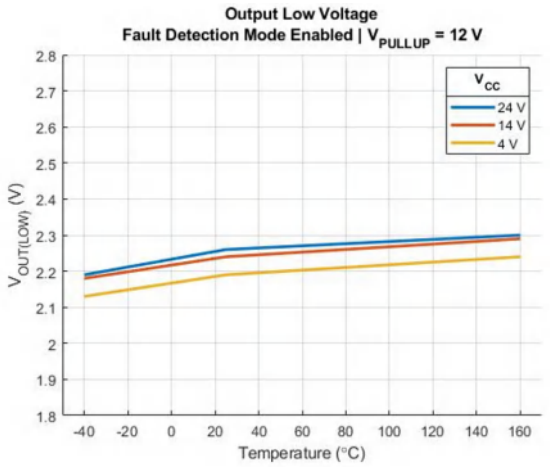

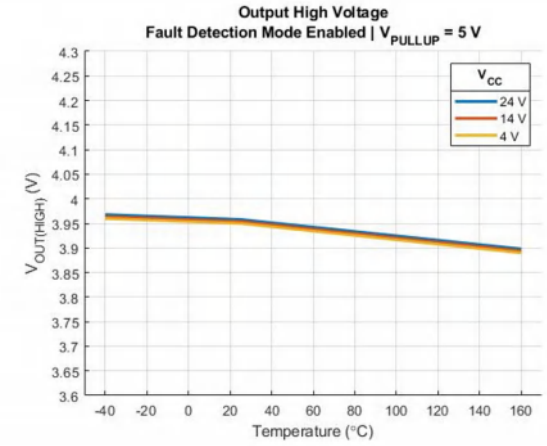

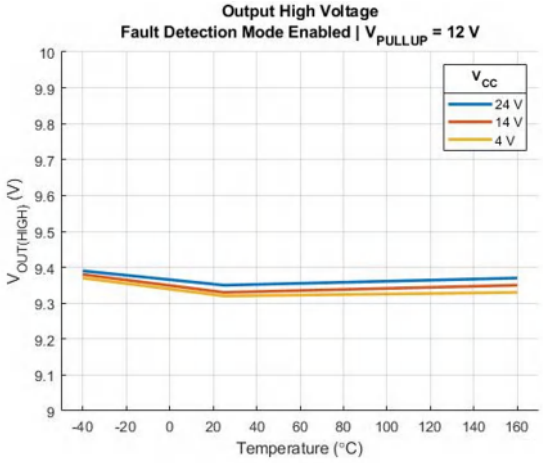

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FUNCTIONAL DESCRIPTION

General

As shown in Figure 5, the A17502 supports three Hall elements that sense the magnetic profile of the ring magnet target simultaneously but at different points (each channel spaced at 1.1 mm pitch), generating two differential internal signals processed for precise switching of the digital output signals. Direction of rotation can be determined based on the phase relationship of the two differential internal signals. The A17502 is intended for use with ring magnet targets, or ferromagnetic targets when properly back-biased.

The Hall-effect sensor IC is self-calibrating and possesses a temperature compensated amplifier as well as a full-range analog-to-digital converter (ADC). This allows for accurate processing of a wide range of target magnetic profile amplitudes and offsets. The on-chip voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect the A17502 due to the stable amplifier design and full-range ADC. The Hall elements and signal processing electronics are integrated on the same silicon substrate.

The A17502 is capable of providing digital information that is representative of the mechanical features of a rotating target. Figure 5 shows the automatic translation of the mechanical profile to the digital output signal. No additional optimization is needed, and minimum processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

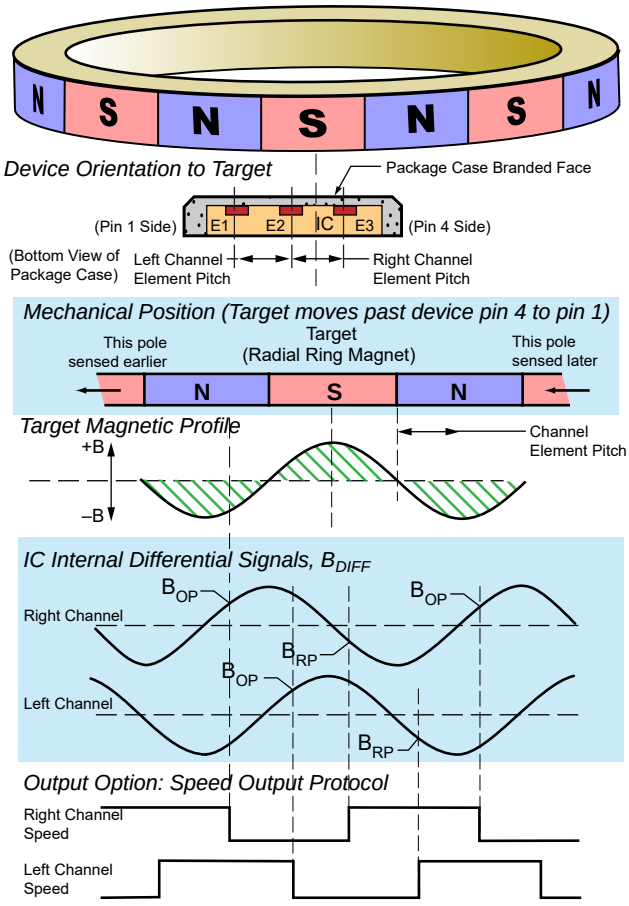

Figure 5: Magnetic Profile and Switch Points (B_{OP} = 70%, B_{RP} = 30%)

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Threshold Algorithm

The A17502 uses a Dynamic Threshold algorithm for determining when to produce an output transition from the magnetic input signal. The threshold set within the sensor IC triggers the output transition when crossed by the digitized magnetic signals (switch point).

With the Dynamic Threshold Algorithm, each switch point is calculated from information learned about the previous target feature. This algorithm allows for robust tracking to produce accurate output transitions for inconsistent magnetic input signals (offset drift, amplitude changes, etc.).

After power-on, the magnetic signal is tracked to find the peaks of the signal. After each new peak is found, the switch points are updated based on a percentage of the previous two peaks.

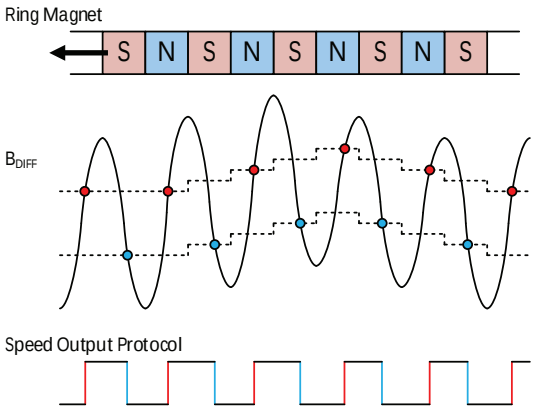

Figure 6: Dynamic Threshold Switch Point Algorithm (B_{OP} = 70%, B_{RP} = 30%)

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Output

The A17502 contains a number of selectable options to change the output protocol or adjust the output behavior. These options allow for the A17502 to be programmed to application-level needs.

Output Protocol

The A17502 contains several programmable output protocols; see Figure 7. These protocols can be programmed for either output pin (OUTA or OUTB) independently. For example, Left Channel Speed can be programmed as the output protocol for OUTA, OUTB, or both output pins.

The A17502 contains two independent signal paths. Most output protocols reference a specific magnetic input signal channel ($B_{DIFF(LEFT)}$ or $B_{DIFF(RIGHT)}$), which is used to determine the output transitions. These channels are determined by the Hall elements used to produce the differential signal, where the left channel differential signal is determined by the left and center element (E1-E2), and the right channel is referenced from the center and right element (E2-E3); see Package Diagram. XOR Speed and Direction output protocols are channel-independent, as both channels are used to determine the output transitions.

For Speed, XOR Speed and Direction output protocols, the polarity of the signal can be inverted by selecting the "Inverse" option of the corresponding protocol. Selecting one of these options will invert the polarity of the output ($V_{OUT(HIGH)}$ and $V_{OUT(LOW)}$) relative to the B_{DIFF} signal(s). For the Pulse output protocols, selecting the "Inverse" option will invert the pulse width for forward and reverse rotation ($t_{w(FWD)}$ and $t_{w(REV)}$).

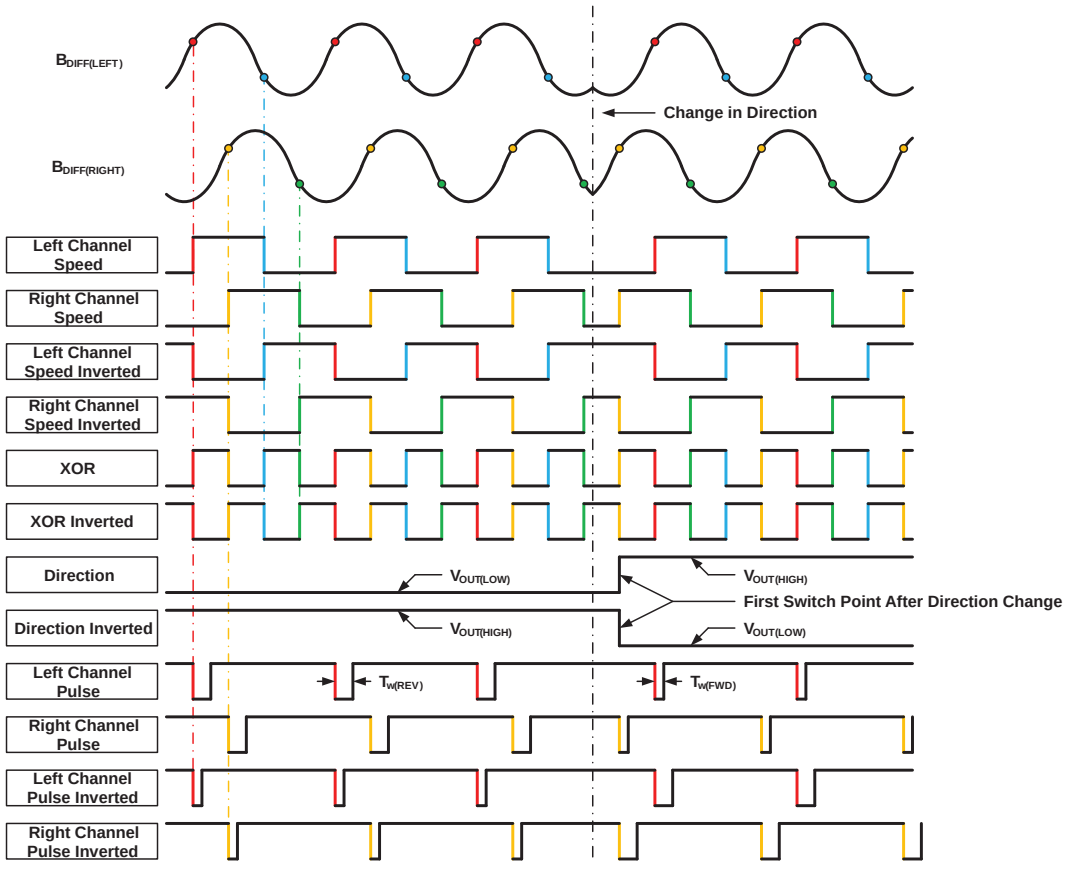

Figure 7: Output Protocol Options

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Fault Detection Mode

The A17502 allows for the output to transition between one of two sets of values. With Fault Detection mode disabled, the output will transition between approximately 0% and 100% of V_{PULLUP}. With Fault Detection mode disabled, the output transitions between approximately 20% and 80% of V_{PULLUP}.

At the beginning of power-on, the A17502 outputs initialize to the V_{PULLUP} level. With Fault Detection mode enabled, the output levels transition from V_{PULLUP} to V_{HIGH} before the end of power-on. After power-on, the output transitions as determined by the programmed algorithm and output protocol between $V_{OUT(HIGH)}$ and $V_{OUT(LOW)}$.

Enabling Fault Detection mode allows for additional communication for cases of open wire or short circuit, as well as allowing for the A17502 to communicate a fault detected from the internal diagnostics. For a typical application load circuit, these cases can be detected by observing either OUTA or OUTB transition to approximately 0 V or V_{PULLUP} after t_{PO}.

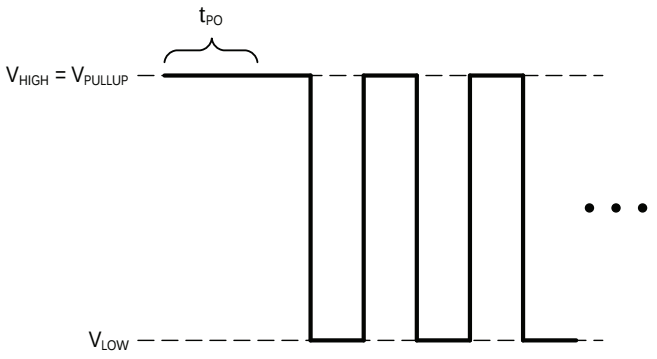

Figure 8: Fault Detection Mode Disabled Output

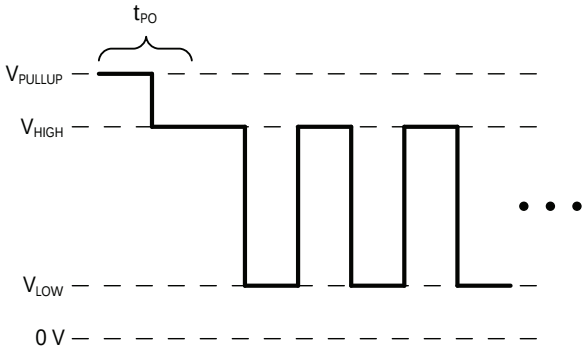

Figure 9: Fault Detection Mode Enabled Output

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Fault Voltage

The A17502 communicates a fault condition by configuring either output to hold within one of three V_{FAULT} ranges (high, mid, and low) for greater than 1 millisecond. Normal operation allows for output transitions to occur over the $V_{FAULT(MID)}$ range; as such, it is necessary to ignore fast transients for less than 1 millisecond through this range.

For internal diagnostics that trigger fault conditions (force the output to go to V_{FAULT}), both outputs will go to the $V_{FAULT(HIGH)}$ range. As there may exist internal or external faults that cause either or both output pins to hold a $V_{FAULT(MID)}$ or $V_{FAULT(LOW)}$ level, these fault ranges should also be monitored. Examples of these fault conditions could be a short circuit of the output to ground, forcing the output to $V_{FAULT(LOW)}$, or a fault in the IC output controller that forces the output to $V_{FAULT(MID)}$.

See Figure 10, Figure 11, and Figure 12 for examples of the output communicating a fault condition.

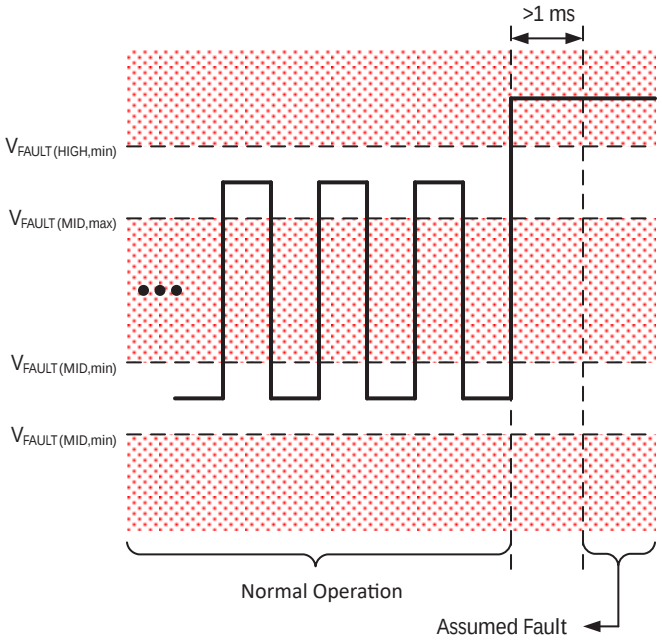

Figure 10: Assumed Fault Example: High Fault

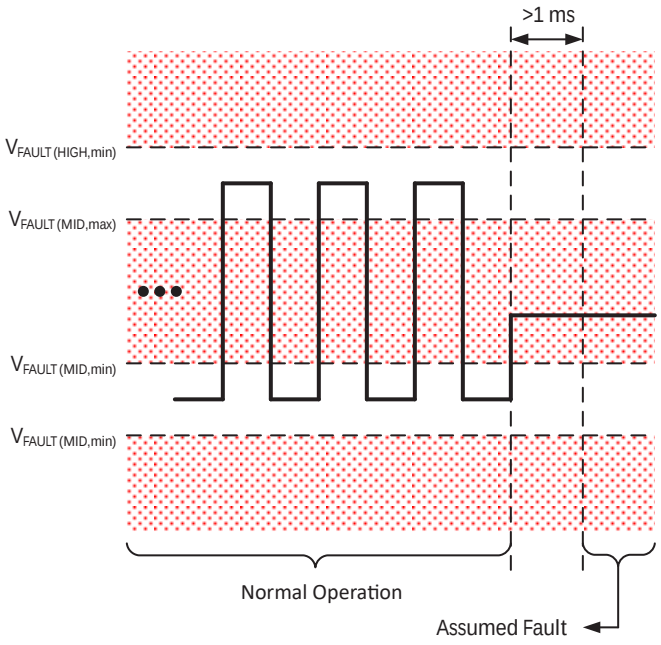

Figure 11: Assumed Fault Example: Mid Fault

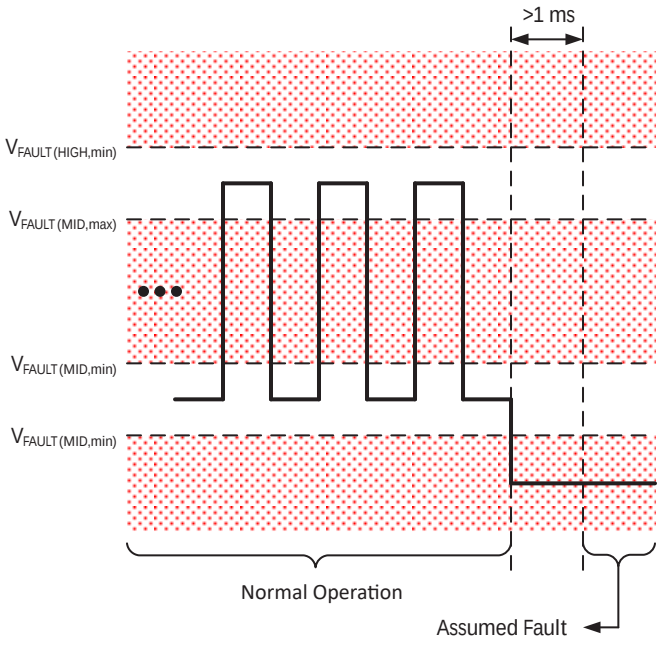

Figure 12: Assumed Fault Example: Low Fault

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DEVICE FEATURES

Undervoltage Lockout

When supply voltage falls below the Undervoltage Lockout voltage ($V_{CC(UV)}$), the A17502 enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. This feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the sensor IC.

Power Supply Protection

The A17502 contains an on-chip regulator and can operate over a wide V_{CC} range. For applications that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection is recommended. Contact Allegro for more information about circuitry to address EMC requirement compliance. Refer to the Typical Application Circuit section.

Startup Hysteresis

With a Power-On and a target held at zero-speed ($f_{OP} \approx 0$ Hz), noise and/or vibration can produce magnetic input signals. Startup hysteresis prevents peak tracking and switch point setting at startup immediately following power-on. This occurs until the sensed differential magnetic signal has moved sufficiently to satisfy the hysteresis band for signal tracking. This feature helps to ensure optimal self-calibration of the magnetic signals by rejecting electrical noise and low-amplitude target vibrations during startup and ensures that calibration occurs on actual target features.

Small Signal Lockout

When $B_{DIFF(pk\text{-}pk)}$ falls below specification, the internal logic of the sensor IC will indicate a reduced signal, as measured in an excessive air gap or a vibration condition. Small Signal Lockout will hold the output state at the level when $B_{DIFF(pk\text{-}pk)}$ was last in-specification. Once $B_{DIFF(pk\text{-}pk)}$ returns to an in-specification value, the output state is released to transition as expected during normal operation. When direction information is not explicitly defined by the selected output protocol, Small Signal Lockout is controlled independently for each channel. For example, Left Channel Speed + Right Channel Speed output protocol will allow for one channel to continue switching while the other is in lockout. When direction information is explicitly communicated, for example XOR + Direction output protocol, Small Signal Lockout will occur when either channel's $B_{DIFF(pk\text{-}pk)}$ falls below specification.

Vibration Robust Signal Tracking

During vibration events, the magnetic input signals can produce oscillations with a sufficient amplitude for the peak tracking algorithms to bound in and produce a non-ideal peak-to-peak. When the A17502 detects a direction change, inward bounding of the peak tracking signals is prevented. This prevents cases of erroneous output transitions from switch points being incorrectly set from vibration signals. Additionally, this allows for immediate acquisition of the magnetic input signals once real target rotation resumes following a vibration event.

Signature Region Robust Signal Tracking

Signature teeth (characterized by an extra target tooth and/or valley) can produce significant variations of the magnetic input signals. The bounded updating of the tracking signals prevent overcompensation for these signature variations to provide robust and accurate switch points for the signature region, as well as the features about the signature region.

Temperature Drift Robust Signal Tracking

As temperature changes can impact both the amplitude and offset of the magnetic signal, a full-range ADC, advanced algorithms, temperature compensation, watchdog timers, and an internal temperature sensor ensure robust signal tracking over temperature.

To compensate for amplitude changes over temperature, temperature compensated gain is first applied to normalize the amplitude over temperature. The full-range ADC and peak tracking algorithms track and acquire the signal to accurately set the switch points.

To compensate for the offset changes over temperature, a unique algorithm implemented to ensure the signal tracking accurately follows and updates the switch points over offset drift. With no target rotation (stopped condition), a watchdog timer is implemented which adjusts the algorithm to track together, allowing for preservation of the correct signal peak-to-peak and switch points once rotation resumes.

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Diagnostics and Fault Reporting

The A17502 contains diagnostics monitors of analog and digital circuits of the IC. These continuously monitor and report if any defect, calculation error, or invalid input stimulus is found. If a diagnostic monitor fires, the outputs of the A17502 will transition to a V_{FAULT} level. For all faults, the outputs will remain at the V_{FAULT} level for enough time to allow the system controller to monitor that a fault has occurred. For some diagnostics, it is possible to clear the fault with a reset of the internal controller of the sensor IC. If any of those diagnostic monitors triggers the fault event, the A17502 will automatically perform a reset of the internal controller after the output is held V_{FAULT} for enough time to allow the system controller to monitor the fault event.

For diagnostics and fault reporting to perform correctly, proper programming and adherence to the specifications and assumptions stated in this datasheet, the A17502 Safety Manual, and any other addendum, corrigendum, and application note that applies to the A17502. For more information on diagnostics and fault reporting, see the A17502 Safety Manual.

Recalibration

Under large amplitude vibration conditions at startup, the peak-to-peak and phase relationship of the magnetic input signals can meet the conditions to calibrate. Once normal rotation resumes, the actual signal amplitudes can be much larger than the peak signals acquired during calibration. Rather than wait several T_{CYCLE} events for the peak signal to be tracked to actual levels, the A17502 will detect the difference and recalibrate on the new signal. Recalibration allows for fast and robust correction from cases of calibration on vibration events.

Pulse Collision Prevention

In cases of “high-speed” vibration, output transitions can occur at very high frequencies, to prevent pulse collision (truncation of the pulse width), the A17502 will prevent output transitions until the current output pulse transition is complete to ensure the system controller can accurately interpret the output signal. This feature is only implemented when a pulse protocol option is selected.

High Configurability

The A17502 contains programmable parameters, as shown in the Selection Guide, that can be configured to provide application-level optimization.

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is a relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, $I_{CC(avg)}$ = 8.5 mA, and $R_{\theta JA}$ = 177°C/W, then:

$$P_D = V_{CC} \times I_{CC(avg)} = 12\ V \times 8.5\ mA = 102\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 102\ mW \times 177°C/W = 18.1°C$$

$$T_J = T_A + \Delta T = 25°C + 18.1°C = 43.1°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

For example, calculating reliability of V_{CC} given observed worst-case ratings, specifically:

T_A = 160°C, $R_{\theta JA}$=177°C/W, $T_{J(max)}$ =175°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 15 mA.

Calculation of the maximum allowable power, $P_{D(max)}$, can be done by first inverting equation 3 and calculating the maximum allowable increase to T_J:

$$\Delta T_{max} = T_{J(max)} - T_A = 175°C - 160°C = 15°C$$

Then, maximum allowable power can be calculated by:

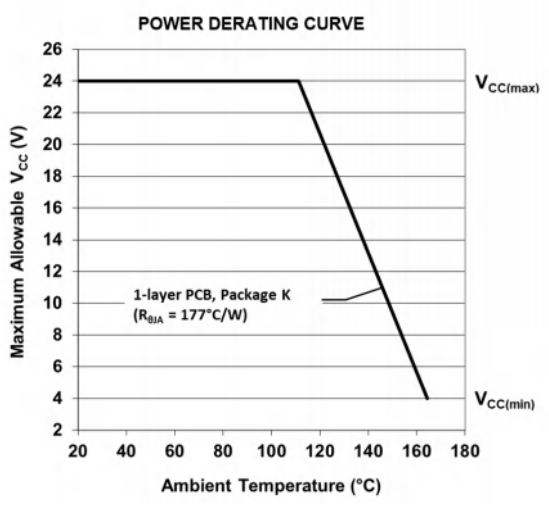
$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 177°C/W = 84.7\ mW$$

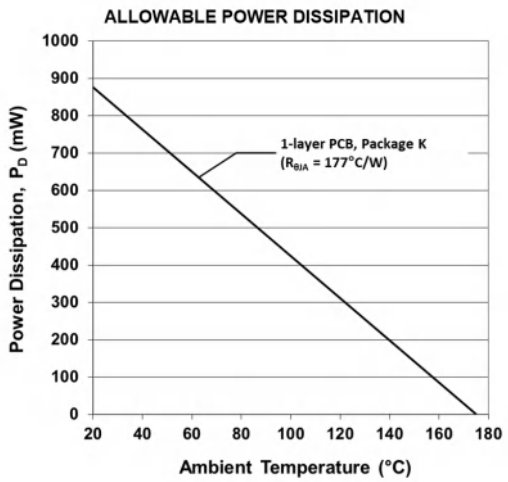
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 84.7\ mW \div 15\ mA = 5.65\ V$$

The results indicate that, at T_A, the application and A17502 can dissipate adequate amounts of heat at voltages less than or equal to $V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.





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PACKAGE OUTLINE DRAWING

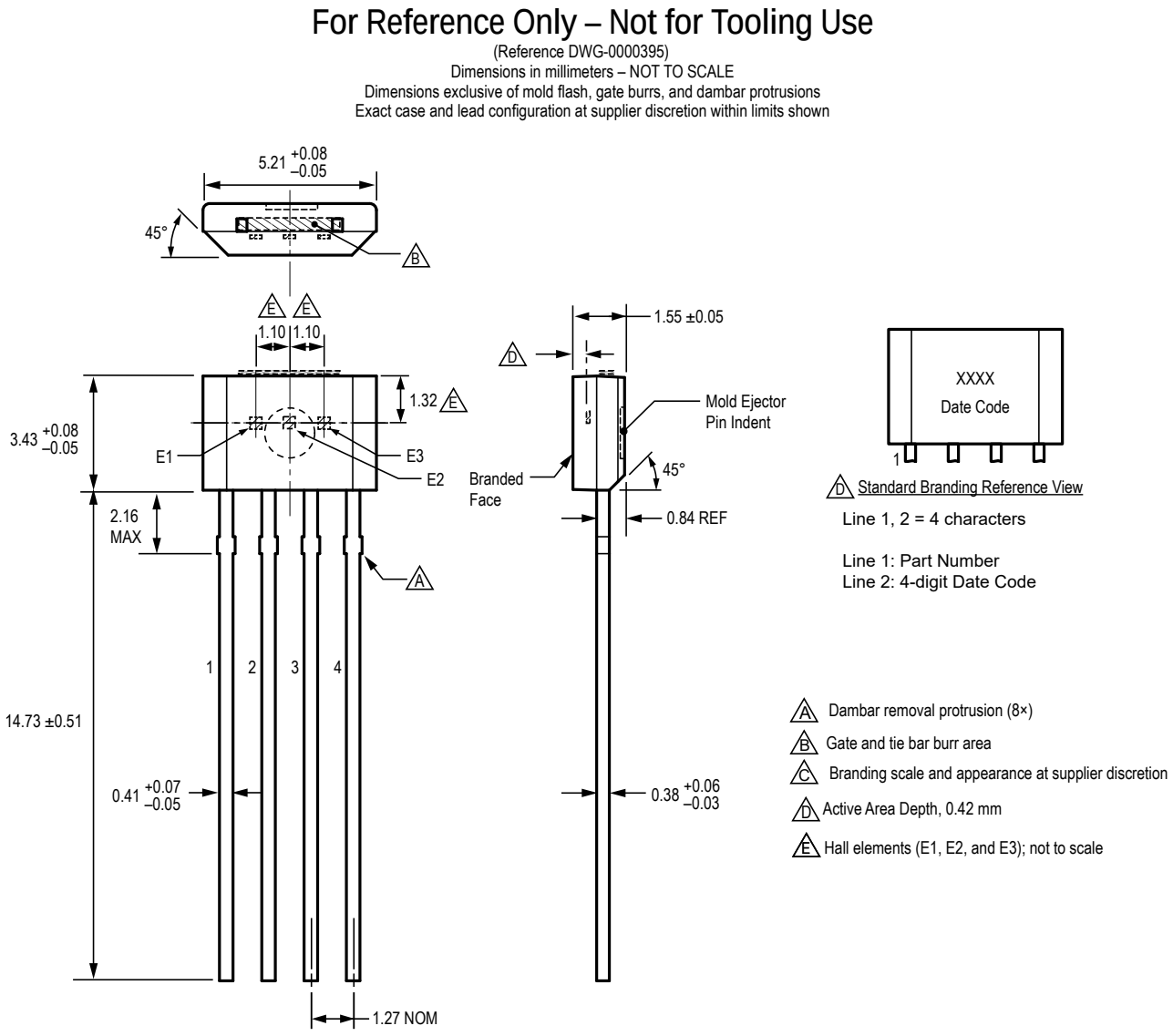

Figure 13: Package K, 4-Pin SIP

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Revision History

Number	Date	Description
–	March 16, 2021	Initial release

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